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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,870	03/31/2004	Kingo Kurotani	501.43663X00	4550

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)	
	10/812,870	KUROTANI ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *6-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 03/31/2004 is acceptable.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/ Restriction

3. Applicant's election without traverse of Species I, **claims 1-5**, in the reply filed on 08/29/2005 is acknowledged.

4. **Claims 6-13** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/29/2005, as noted above.

Specification

5. The disclosure is objected to because of the following informalities: typographical on line 8, page 8, which is 14(b), which should be 15(b).

Appropriate correction is required.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-3** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Leong U.S. Patent 6,372,557 (the '557 reference).

The '557 reference discloses in the figures, particularly Fig. 3L, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device, comprising a laterally diffused field effect transistor including, over a semiconductor substrate (102), an element-forming area and a scribing area (not shown) surrounding the element-forming area, the transistor including:

(a) a semiconductor layer (104, column 3, first paragraph) of a first conductive type (p) formed in the element-forming area over the semiconductor substrate (102),

(b) a gate insulating film (108, column 3, lines 12-16) formed over the semiconductor layer,

(c) a gate electrode (110a or 110b, column 3, lines 20-22) formed over the gate insulating film,

(d) a source (126/120) comprised of a first semiconductor region (126, column 3, lines 20-67, particularly lines 53-55 and 65-67) of a second conductive type (n) which is different from the first conductive type (p),

(e) a drain (130/132) comprised of a second semiconductor region (132, column 4, lines 3-7, "lightly doped drain region") of the second conductive type (n) having a first impurity concentration, and a third semiconductor region (130) of the second conductive type having a higher second impurity concentration than the first impurity concentration ("lightly doped") and being formed at a position farther from the gate electrode than the second semiconductor region,

(f) a fourth semiconductor region of the first conductive type (p) where a channel region (no number, generally formed between the source and the drain) is formed,

(g) an electrode (138) electrically connected (through semiconductor substrate 102, p+++ region 100, sinker 122, metal pad 136a, and to the source (126/120) to the source and formed over the rear surface of the semiconductor substrate, and

(h) a source electrode pad (136a, "electrode pad" is interpreted broadly) formed in the element-forming area over the front surface of the semiconductor substrate and being electrically connected to the semiconductor substrate.

However, the reference does not disclose the claimed functional limitation that the source electrode pad (136a) is for evaluation. Nevertheless, the semiconductor device including the

source electrode pad, at some point during its lifetime, should be tested and evaluated for its functionality; hence the limitation "for evaluation" appears to be inherent, specifically with the disclosure of the reference that "[A]fter testing, the wafer is cut into individual transistors" (column 4, lines 53-55).

In the alternative, the source electrode pad could be used for evaluation as the reference does not exclude all its possible usage.

Referring to **claim 2**, the '557 reference does not disclose that the source electrode pad for evaluation is formed in the scribing area, which is for all practical purposes, the same as the claimed limitation the source electrode pad for evaluation is not formed in the scribing area.

Referring to **claim 3**, the '557 reference further discloses that the source electrode pad (136a) for evaluation or could be for evaluation and the semiconductor substrate (102) are connected to each other through a fifth semiconductor region (100/122 or 122) of the first conductive type (p) formed in the semiconductor layer (104).

7. **Claims 1-3** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Yasuhara et al. U.S. Patent Application Publication 20020167047 (the '047 reference).

The '047 reference discloses in Figs. 29 and 38 and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device, comprising a laterally diffused field effect transistor including, over a semiconductor substrate (771), an

element-forming area and a scribing area (not shown) surrounding the element-forming area, the transistor including:

(a) a semiconductor layer (772, paragraph [0194]) of a first conductive type (p) formed in the element-forming area over the semiconductor substrate (771),

(b) a gate insulating film (776, paragraph [0195]) formed over the semiconductor layer,

(c) a gate electrode (777b) formed over the gate insulating film,

(d) a source (774) comprised of a first semiconductor region of a second conductive type (n) which is different from the first conductive type (p),

(e) a drain (778/775) comprised of a second semiconductor region (775) of the second conductive type (n) having a first impurity concentration (n), and a third semiconductor region (778) of the second conductive type having a higher second impurity concentration (n+) than the first impurity concentration (n) and being formed at a position farther from the gate electrode than the second semiconductor region,

(f) a fourth semiconductor region of the first conductive type (p) where a channel region (no number, generally formed between the source and the drain) is formed,

(g) an electrode (785) electrically connected to the source and formed over the rear surface of the semiconductor substrate (paragraph [0199]), and

(h) a source electrode pad (782, "electrode pad" is interpreted broadly) formed in the element-forming area over the front surface of the semiconductor substrate and being electrically connected to the semiconductor substrate.

However, the reference does not disclose the claimed functional limitation that the source electrode pad (782) is for evaluation. Nevertheless, the semiconductor device including the

source electrode pad, at some point during its lifetime, should be evaluated for its functionality; hence the limitation "for evaluation" appears to be inherent.

Referring to **claim 2**, the '047 reference does not disclose that the source electrode pad, which could be for evaluation, is formed in the scribing area, which is for all practical purposes, the same as the claimed limitation the source electrode pad for evaluation is not formed in the scribing area.

Referring to **claim 3**, the '047 reference further discloses that the source electrode pad (782), which could be for evaluation, and the semiconductor substrate (771) are connected to each other through a fifth semiconductor region (780a) of the first conductive type (p) formed in the semiconductor layer (772).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claim 4** is rejected under 35 U.S.C. §103(a) as being unpatentable over Leong U.S. Patent 6,372,557 (the '557 reference).

The '557 reference discloses a semiconductor device as claimed and as detailed above for claim 1 and further discloses that a passivation film (134) is formed over the semiconductor substrate and the thickness from the rear surface of the semiconductor substrate to the front surface of the passivation film covering ("covering" is interpreted broadly, in a similar manner that

passivation layer film 16 is covering the electrode pads 12a or 15a, Fig 3, present invention) the source electrode pad is the combined thickness of the thickness of the semiconductor substrate 102, the thickness of layer 104, the thickness of gate oxide 108, and the thickness of the passivation film 134.

However, the reference does not appear to disclose that the combined thickness is about 200 μm or less.

Nevertheless, the reference discloses that the thickness of the substrate 102, after a thinning process, is about 152.4 μm (6 mils, column 4, lines e42-48), the thickness of layer 104 is about 9 μm (column 3, lines 1-2), the thickness of gate oxide 108 of about 0.080 μm (80 nm, column 3, lines 14-17), and does not disclose a thickness for the passivation oxide layer 134. Although the reference does not disclose a thickness for the passivation oxide layer 134, the thickness of the passivation oxide layer 134, although not to scale, is comparable to the thickness of the gate oxide, which is about 0.080 μm, and at most comparable to the thickness of layer 104, which is about 9 μm. Hence, the combined thickness appears to be about 200 μm or less as claimed.

9. **Claim 4** is rejected under 35 U.S.C. §103(a) as being unpatentable over Yasuhara et al. U.S. Patent Application Publication 20020167047 (the '047 reference).

The '047 reference discloses a semiconductor device as claimed and as detailed above for claim 1 and further discloses that a passivation film (783, paragraph [0209], "passivation film" is interpreted broadly) is formed over the semiconductor substrate and the thickness from the rear surface of the semiconductor substrate to the front surface of the passivation film covering the

source electrode pad is the combined thickness of the thickness of semiconductor substrate 771, the thickness of layer 772, the thickness of the first insulation layer 783, and the thickness of the passivation film 783.

However, the reference does not appear to disclose that the combined thickness is about 200 μm or less.

Nevertheless, the reference discloses that the thickness of the substrate 771 is about 100 μm (paragraph [0210]), the thickness of layer 772 is about 3 μm (paragraph [0194]), the thickness of said first insulation layer 783 is about 1 μm or more (paragraph [0209]), and the thickness for the passivation insulation layer 134 is also about 1 μm or more. Therefore, by law one can not say for certain that the combined thickness of "100 μm, 3 μm, twice 1 μm or more" is the same as "200 μm or less" as claimed. However, the reference also teaches in paragraph [0209] that there shall be an upper limit to the "1 μm or more" thickness; hence, one of ordinary skill in the art at the time the invention was made would be motivated to keep the "1 μm or more" thickness as thin as possible (to save material) and also because there is an upper limit to the "1 μm or more" thickness. Consequently, the combined thickness of "100 μm, 3 μm, twice 1 μm or more" appears to be about 200 μm or less as claimed.

Allowable Subject Matter

10. **Claim 5** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device as recited in claim 5, characterized in that a drain electrode pad is formed over the front surface of the semiconductor substrate and is electrically connected to the third semiconductor region, and that a gate electrode pad is electrically connected to the gate electrode.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
October 12, 2005